

## ***REMARKS***

Applicants thank the Examiner for the very thorough consideration given the present application.

Claims 1-13 are now present in this application. Claims 1, 7 and 13 are independent.

Reconsideration of this application is respectfully requested.

### ***Information Disclosure Statement***

Applicants respectfully notify the Examiner that they filed an Information Disclosure Statement subsequent to the mailing of the outstanding Office Action of August 1, 2005 and ask the Examiner to take into consideration the references cited in the IDS in the examination of this Application. Furthermore, Applicant's below-named representative obtained a computer-generated translation of one of the references cited in the IDs, i.e., of JP 2002-289653, and a copy of that translation is attached hereto for the convenience of the Examiner.

### ***Restriction Requirement***

Applicants continue to traverse the restriction requirement, argue that it is improper for a number of reasons, and hereby request that the restriction

requirement be withdrawn and claims 7-12 be examined on their merits. Those reasons are set forth in the Amendment filed on May 9, 2005 and in a Petition to the Commissioner under 35 USC §181 and §1.144 filed on even date herewith, the substance of both papers being hereby incorporated by reference herein.

*Rejections under 35 U.S.C. §102*

Claims 1 and 13 stand rejected under 35 U.S.C. §102(b) as clearly anticipated by U.S. Patent 5,390,080 to Melton et al. ("Melton"). This rejection is respectfully traversed.

During patent examination the PTO bears the initial burden of presenting a *prima facie* case of unpatentability. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984).

If the PTO fails to meet this burden, then the applicant is entitled to the patent. However, when a *prima facie* case is made, the burden shifts to the applicant to come forward with evidence and/or argument supporting patentability. Patentability *vel non* is then determined on the entirety of the record, by a preponderance of evidence and weight of argument, *Id.*

A prior art reference anticipates the subject matter of a claim when that reference discloses every feature of the claimed invention, either explicitly or inherently. In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431

(Fed. Cir. 1997) and Hazani v. Int'l Trade Comm'n, 126 F.3d 1473, 1477, 44 USPQ2d 1358, 1361 (Fed Cir. 1997). While, of course, it is possible that it is inherent in the operation of the prior art device that a particular element operates as theorized by the Examiner, inherency may not be established by probabilities or possibilities. In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (CCPA 1981) and In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993). In this regard, Applicants respectfully note that there can be no speculation or only possibilities involved in a holding of inherency. What is alleged to be inherent must necessarily occur. The mere fact that something *may* result from a given set of circumstances is not sufficient. In re Oelrich, 212 USPQ 323, 326 (CCPA 1991). “Inherent anticipation requires that the missing descriptive material is ‘necessarily present,’ not merely probably or possibly present, in the prior art.” Trintec Indus., Inc. v. Top-U.S.A. Corp., 295 F.3d 1292, 1295, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002) (quoting In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)).

Melton’s barrier layer 24 is not disclosed as having a plurality of pores, as recited. In fact, Melton discloses just the opposite. In col. 4, lines 18-25, Melton discloses that its barrier layer (first layer) “. . . provides a zinc-free barrier between the copper and the zinc alloy that does not contain voids . . .”

Nor does Melton disclose “a tin layer plated on the barrier layer, and alloyed with a portion of the copper foil . . . through the pores,” as recited in claim 1.

The only plated layer disclosed by Melton is the barrier layer (first layer) 24 – see col. 4, lines 41-44 of Melton. Melton’s tin layer 26 is disclosed as a solder paste applied to the first (barrier) layer 24 by screen printing – see col. 3, lines 25-41. Moreover, because Melton explicitly discloses that its barrier layer 24 has no voids (pores), Melton’s tin-zinc layer 26 is not alloyed through the non-existent pores. Additionally, Melton discloses, in the paragraph bridging cols. 3 and 4, that the first (barrier) layer 24 remains solid to prevent contact between the copper pad and the zinc-tin liquid (26).

Applicants also respectfully submit that the statement that the materials used for alloy layer 24 of Melton can be chosen depending upon the void volume desired has not been explained to be relevant to a rejection under 35 U.S.C. §102(b), which requires anticipation and is not concerned with the obviousness of selecting materials used for alloy layer 24. Moreover, because Melton expressly discloses that its barrier layer 24 does not contain voids, the desired void volume of Melton is zero.

Accordingly, Melton does not anticipate claim 1 or claim 13.

Reconsideration and withdrawal of this rejection of claims 1 and 13 under 35 U.S.C. §102(b) are respectfully requested.

Rejections under 35 U.S.C. §103

Claims 1 and 4-6 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U. S. Patent 5,390,080 to Melton et al. ("Melton"). This rejection is respectfully traversed.

A complete discussion of the Examiner's rejection is set forth in the Office Action, and is not being repeated here.

The Office Action asserts that Melton is silent about the pore density of the alloy layer. Applicants respectfully disagree with this statement. As noted above, Melton's barrier layer is expressly taught to have no voids. Because the claimed invention recites a barrier layer with pores, Melton cannot anticipate or render obvious the invention recited in claims 1 and 4-6.

With respect to claims 5 and 6, Melton does not disclose particular thicknesses of layers 24 or 26 and, therefore, does not provide any motivation to make those layers of the specific claimed thickness range.

It is well settled that a rejection under 35 U.S.C. §103 cannot properly be based on speculation but must be based on objective factual evidence of record. See, In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968). See, also, In re GPAC, Inc., 35 USPQ2d

1116 at 1123 (Fed. Cir. 1995) and Ex parte Haymond, 41 USPQ2d 1217 at 1220 (Bd. Pat. App. & Int. 1996).

A factual inquiry whether to modify a reference must be based on objective evidence of record, not merely conclusory statements of the Examiner. See, In re Lee, 277 F.3d 1338, 1343, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002).

Moreover, allegations of motivation to modify a reference that are in the form of broad generic conclusions unsupported by objective factual evidence and, standing alone, are not “evidence” of proper motivation to combine these references. See In re Dembiczak, 175 F.3d 994 at 1000, 50 USPQ2d 1614 at 1617 (Fed. Cir. 1999).

Additionally, a rejection must be based on objective factual evidence rather than mere conclusory statements by an Examiner, See, In re Lee, 277 F.3d 1338, 1343, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002).

The conclusion that the aforementioned claimed thickness features are an obvious matter of design choice is nothing more than speculation that fails to provide any objective, factual evidence of why a skilled worker would be motivated to provide such modifications, as required by existing case law, such as, for example, In re Lee, cited above.

This rejection improperly establishes a rule that claimed thickness ranges are *per se* obvious. As stated by the Federal Circuit in In re Ochiai, 71 F.3d 1565, 1572, 37 USPQ2d 1127, 1133 (Fed. Cir. 1995), “reliance on *per se*

rules of obviousness is legally incorrect and must cease.” For a *prima facie* case of obviousness to be established, the teachings from the prior art itself must appear to have suggested the claimed subject matter to one of ordinary skill in the art. *See In re Rinehart*, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976). The mere fact that the prior art could be modified as proposed by the Examiner is not sufficient to establish a *prima facie* case of obviousness. *See In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992). The Examiner must explain why the prior art would have suggested to one of ordinary skill in the art the desirability of the modification. *See Fritch*, 972 F.2d at 1266, 23 USPQ2d at 1783-84.

The Office Action fails to properly explain why the prior art would have suggested to one of ordinary skill in the art the desirability of modifying Melton to arrive at the claimed layer thickness ranges.

Reconsideration and withdrawal of this rejection of claims 1 and 4-6 is respectfully requested.

**Allowable Subject Matter**

The Examiner states that claims 2 and 3 would be allowable if rewritten in independent form.

Applicants thank the Examiner for the early indication of allowable subject matter in this application. Claim 2 depends from independent claim 1, and claim 3 depends from claim 2 and are therefore allowable based on their dependence from claim 1 which is believed to be allowable. Accordingly, claims 2 and 3 have not been rewritten in independent form.

*Additional Cited References*

Because the remaining references cited by the Examiner have not been utilized to reject the claims, but have merely been cited to show the state of the art, no comment need be made with respect thereto.

*Conclusion*

All of the stated grounds of restriction and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding restrictions and rejections and that they be withdrawn, and claims 1-13 be examined on their merits and allowed. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone Robert J. Webster, Registration No. 47,472, at (703) 205-8000, in the Washington, D.C. area.

Prompt and favorable consideration of this Amendment is respectfully requested.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachment: JPO Computer-generated English language translation of  
JP 2002-289653

## \* NOTICES \*

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## CLAIMS

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### [Claim(s)]

[Claim 1] The tape career for semiconductor devices characterized by forming a tin-copper alloy layer with a thickness of 0.20 micrometers or more and a pure tin layer with a thickness of 0.15-0.80 micrometers by performing noble-metals plating, such as silver, gold, and palladium, applying a solder resist to the position except a part for the terminal area of said circuit pattern, and forming and heat-treating a tinning layer to a part for said terminal area on the circuit pattern of the copper foil given through the adhesives layer on the insulating film.

[Claim 2] The tape career for semiconductor devices according to claim 1 characterized by setting thickness of said noble-metals plating to 0.1 micrometers or less in the tape career for semiconductor devices according to claim 1.

[Claim 3] On the circuit pattern of the copper foil given through the adhesives layer on the insulating film By applying a solder resist to the position except a part for the terminal area of said circuit pattern, after performing noble-metals plating, such as silver, gold, and palladium, forming a tinning layer in a part for said terminal area after that, and heat-treating after that The manufacture approach of the tape career for semiconductor devices characterized by forming a tin-copper alloy layer with a thickness of 0.20 micrometers or more and a pure tin layer with a thickness of 0.15-0.80 micrometers.

[Claim 4] The manufacture approach of the tape career for semiconductor devices characterized by setting thickness of said noble-metals plating to 0.1 micrometers or less in the manufacture approach according to claim 3.

[Claim 5] The manufacture approach of the tape career for semiconductor devices characterized by performing said tinning with nonelectrolytic plating in the manufacture approach according to claim 3 or 4.

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[Translation done.]

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## DETAILED DESCRIPTION

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### [Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the tape career and the tinning technique of a tape career for semiconductor devices like the TAB tape career which is precision electronic parts, and the structure which faced performing tinning to the circuit pattern of the copper foil especially, and prevented \*\*\*\*\* of the copper in the solder resist case.

[0002]

[Description of the Prior Art] The structure of the conventional TAB tape career forms the predetermined circuit pattern 3 in the copper foil stuck on the insulation film 1 made of polyimide resin through the adhesives layer 2, as shown in drawing 2 ( drawing 2 (a) ). On the circuit pattern 3, at the position except parts for a terminal area, such as the copper lead 3a Carry out printing spreading of the solder resist 6 as an insulating layer ( drawing 2 R> 2 (b) ), and after that, in order to give the junction nature stabilized in copper lead 3a which is a part for the terminal area of the circuit pattern 3 concerned It is the structure ( drawing 2 (d) ) which formed the pure tinning layer 4 by non-electrolyzed tinning ( drawing 2 (c) ), and formed the tin-copper alloy layer 5 by heat-treatment.

[0003] As shown in drawing 3 , a semiconductor device (IC chip) 7 is arranged so that it may be located in a device hole, and after the mounting activity to the semiconductor device of this TAB tape career carries out alignment of the electrode of a semiconductor device 7 to the inner lead projected in the device hole, it is stuck by pressure with a bonding tool. The golden bump 8 is formed in the electrode of a semiconductor device 7, if it is stuck to copper lead 3a by pressure in the condition of having been heated, tinning will fuse, a golden-tin alloy will form and an inner lead will be joined to an electrode.

[0004]

[Problem(s) to be Solved by the Invention] Generally, since tinning is excellent in corrosion resistance and soldering nature, it is widely used for electronic parts.

[0005] However, in the above-mentioned conventional TAB tape career, in case non-electrolyzed \*\*\*\*\* is carried out, as shown in drawing 4 R> 4 , in the case of the lower part of a solder resist 6, copper carries out the superfluous dissolution in the section (edge), the part (superfluous dissolution section 9) corroded to copper lead 3a at the groove is formed, and there is a problem of reducing lead reinforcement.

[0006] Although non-electrolyzed tinning generally deposits in a permutation with copper, the pretreatment liquid of non-electrolyzed tinning cannot permeate easily in this case, the residue of the organic substance, a contamination, etc. remain in a copper front face, a reaction rate becomes early remarkably at the time of non-electrolyzed tinning, and copper dissolves a solder resist lower part superfluously.

[0007] A difference arises in a reaction rate at the time of non-electrolyzed tinning in the large place of plating area since the demand of the formation of a detailed circuit pattern is strong recently and plating area is furthermore smaller, and a detailed part. Especially, in the detailed section, the reaction rate of non-electrolyzed tinning becomes early, copper carries out the superfluous dissolution, and lead

reinforcement falls.

[0008] As other troubles, since it is known well that whiskers (mustache-like crystal) will generate it if a tinning coat is left immediately after tinning and generating of whiskers becomes a short cause by the pattern of a detailed pitch especially, various examination has been performed. As a control means of these tin whiskers, it is (1). As substrate plating, a nickel, copper, lead, solder, tin-nickel alloy, and tin-copper alloy layer is formed. (2) Perform reflow processing after plating. (3) Heat after plating and perform annealing treatment. \*\* is known.

[0009] However, the above (1) Since a substrate plating process is given, as for the technique of performing substrate plating, cost becomes high. Above (2) Even if the method of performing reflow processing after plating performs thick uniform plating first, variation arises in plating thickness and the problem that a tinning front face oxidizes further produces after a reflow. Although the approach of performing annealing treatment after the plating of the above (3) has whiskers depressor effect for a short period of time, since growth of whiskers cannot be completely prevented if the long period of time of about six months comes, there is a problem that it does not become a perfect cure against whiskers.

[0010] Then, the purpose of this invention is to offer the tape career for semiconductor devices and its manufacture approach of the tinning structure that the whiskers of tinning can be controlled cheaply, without spoiling the property of tinning and of having high dependability while it solves the above-mentioned technical problem and prevents \*\*\*\*\* of the superfluous dissolution of the copper of lead wiring of a solder resist lower part, i.e., the copper in the solder resist case.

[0011]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, this invention is constituted as follows.

[0012] (1) The tape career for semiconductor devices concerning invention of claim 1 On the circuit pattern of the copper foil given through the adhesives layer on the insulating film By performing noble-metals plating, such as silver, gold, and palladium, applying a solder resist to the position except a part for the terminal area of said circuit pattern, and forming and heat-treating a tinning layer to a part for said terminal area It is characterized by forming a tin-copper alloy layer with a thickness of 0.20 micrometers or more and a pure tin layer with a thickness of 0.15-0.80 micrometers.

[0013] (2) Invention of claim 2 is characterized by setting thickness of said noble-metals plating to 0.1 micrometers or less in the tape career for semiconductor devices according to claim 1.

[0014] (3) The manufacture approach of the tape career for semiconductor devices concerning invention of claim 3 On the circuit pattern of the copper foil given through the adhesives layer on the insulating film By applying a solder resist to the position except a part for the terminal area of said circuit pattern, after performing noble-metals plating, such as silver, gold, and palladium, forming a tinning layer in a part for said terminal area after that, and heat-treating after that It is characterized by forming a tin-copper alloy layer with a thickness of 0.20 micrometers or more and a pure tin layer with a thickness of 0.15-0.80 micrometers.

[0015] (4) Invention of claim 4 is characterized by setting thickness of said noble-metals plating to 0.1 micrometers or less in the manufacture approach according to claim 3.

[0016] (5) In the manufacture approach according to claim 3 or 4, it is characterized by performing said tinning with nonelectrolytic plating.

[0017]

[Embodiment of the Invention] Hereafter, this invention is explained based on the operation gestalt of illustration.

[0018] The manufacture approach of the TAB tape career as an example of the tape career for semiconductor devices by this invention is shown in drawing 1. First, by performing etching, after making the photo mask which has a predetermined wiring lead pattern after applying a predetermined photoresist to the tape career which formed copper foil through the adhesives layer 2 on the insulation film 1 made of polyimide resin and drying it let pass and expose and develop, as shown in drawing 1 (a), the predetermined detailed circuit pattern 3 is produced.

[0019] Next, as shown in drawing 1 (b), the noble-metals plating layers 10, such as silver with a

thickness of 0.01-0.1 micrometers, gold, and palladium, are formed on the circuit pattern 3 of this copper foil.

[0020] Subsequently, as shown in drawing 1 (c), a solder resist 6 is applied to the part on the circuit pattern 3 with which this noble-metals plating layer 10 was formed, i.e., the position except parts for a terminal area, such as copper lead 3a, by print processes.

[0021] As shown in drawing 1 (d), next, to a part for the above-mentioned terminal area of this tape career (copper lead 3a etc.) That is, by forming the tinning layer 4 on the noble-metals plating layer 10, and carrying out 100-150 degrees C and heat-treatment for 5 minutes - 90 minutes after that Copper is diffused in the tinning layer concerned, and as shown in drawing 1 R> 1 (e), the copper diffusion tinning layer, the tinning layer 4, i.e., the pure tin layer, with a thickness of 0.15-0.80 micrometers which does not contain copper substantially, 5 with a thickness of 0.20 micrometers or more, i.e., a tin-copper alloy layer, is formed.

[0022] Thus, the noble-metals plating layers 10, such as silver, gold, and palladium, are formed previously, parts for a terminal area, such as copper lead 3a, are covered with this noble-metals plating layer 10, and, as for the TAB tape career formed, a solder resist 6 is formed on it. For this reason, since the copper front face is covered with the noble-metals plating layer 10 and copper foil does not contact plating liquid even if plating liquid trespasses upon the inferior surface of tongue of a solder resist 6 in the case of tinning processing, local electric corrosion does not happen. Therefore, the superfluous dissolution section 9 of the copper shown in drawing 4 is not formed in copper lead 3a. Therefore, it can lose un-arranging [ that the copper superfluous dissolution section 9 exists in copper lead 3a, and the reinforcement of copper lead 3a becomes weaker ].

[0023] As for the thickness of the noble-metals plating layer 10, in the above-mentioned manufacture approach of a TAB tape career, it is desirable that it is 0.1 micrometers or less. It is because the whole surface is covered and carries out stripes with noble-metals plating mostly, time amount will be taken before non-electrolyzed tinning liquid attains even the copper of a substrate through a pinhole and a deposit rate will fall, in case it deposits through the pinhole of a noble-metals plating coat at the time of non-electrolyzed tinning if the thickness of this noble-metals plating layer 10 exceeds 0.1 micrometers.

[0024] if the reason for having set thickness of the pure tin layer 4 to 0.15-0.80 micrometers becomes difficult [ the bonding nature of an inner lead ] in the case of less than 0.15 micrometers on the other hand and 0.8 micrometers is exceeded -- plating -- it is because who is produced and it becomes the cause of a short circuit. Moreover, the reason for having set thickness of the tin-copper alloy layer 5 by the 2nd tinning processing to 0.20 micrometers or more is that whiskers depressor effect becomes inadequate in the case of less than 0.20 micrometers.

[0025] As shown in drawing 3 , a semiconductor device (IC chip) 7 is arranged so that it may be located in a device hole, and after the mounting activity to the semiconductor device of the above-mentioned TAB tape career carries out alignment of the electrode of a semiconductor device 7 to the inner lead projected in the device hole, it is stuck by pressure with a bonding tool. The golden bump 8 is formed in the electrode of a semiconductor device 7, if it is stuck to copper lead 3a by pressure in the condition of having been heated, tinning will fuse, a golden-tin alloy will form and an inner lead will be firmly joined to an electrode.

[0026]

[Example] After making the photo mask which has a predetermined wiring lead pattern after applying a predetermined resist to the tape career of 25 micrometers of copper foil formed through the adhesives layer 2 on the insulation film 1 made of polyimide resin and drying it let pass and expose and develop, the lead pattern was produced by performing etching.

[0027] And first, on the copper circuit pattern of the tape career for semiconductor devices with which the copper detailed pattern was formed on the insulation film 1 made of polyimide resin, after performing silver plating with a thickness of 0.01-0.25 micrometers and printing a solder resist 6 to the part on the circuit pattern, about 0.5-micrometer tinning layer was formed and the pure tin layer 4 and the tin-copper alloy layer 5 were formed by heat-treatment at 100 degrees C - 150 degrees C for 5 minutes - 90 minutes. Here, the thing in which 0.2-0.3 micrometers and 0.15-0.20 micrometers of tin-

copper alloy layers 5 were made to form the pure tin layer 4 by heat-treatment was produced.

[0028] Although tinning could be formed by the approach of either electrolysis and nonelectrolytic plating, it was taken as nonelectrolytic plating at the point with little variation in plating thickness here.

[0029] Non-electrolyzed tinning liquid was processed in 70 degrees C and 5-500s using ISHIHARA CHEMICAL 580M. Thus, about the produced sample, copper superfluous soluble evaluation was performed by cross-section observation. This result is shown in Table 1 as tinning conditions and an overcopper solubility evaluation result.

[0030]

[Table 1]

スズめっき条件と銅過剰溶解性評価結果

サンプル	1回目Agめっき厚	2回目めっき厚		銅過剰溶解性評価結果
		合金層厚	純スズ厚	
1	0	0.22	0.35~0.4	×
2	0.01	0.22	0.25~0.3	○
3	0.05	0.22	0.25~0.3	○
4	0.10	0.22	0.25~0.3	○
5	0.15	0.18	0.15~0.2	○
6	0.20	0.15	0.10~0.15	○

[0031] As shown in Table 1, as for the superfluous dissolution of copper, neither of the samples which carried out Ag plating to the substrate was observed. That is, it is thought that the superfluous dissolution of copper can prevent it if the thickness of a silver plating layer (noble-metals plating layer 10) is at least 0.01 micrometers or more. Moreover, since the deposit rate of tinning will fall if silver plating thickness exceeds 0.1 micrometers, silver plating thickness has desirable 0.1 micrometers or less.

[0032] The superfluous dissolution of copper was observed at the case which carried out non-electrolyzed tinning after solder resist printing like a sample 1 on the other hand.

[0033] Next, about 150 inner leads after measuring pure tinning thickness with a KOKURU meter, measuring all tin thickness by the fluorescence-X-rays thickness gage, deducting and carrying out (pure tin thickness) from (all tin thickness) and asking for and carrying out neglect of the thickness of a tin-copper alloy layer in one to June (30 days, 60 days, 90 days, 180 days), whiskers were observed with the 200 times as many optical microscope as this, respectively, and the occurrences of the whiskers were counted. This tinning condition, tinning thickness, and a whiskers nature evaluation result are shown in Table 2. It was observed that whiskers occurrences increase as shown in Table 2 and lapsed days increased, when a tin-copper alloy layer was less than (samples 2, 5, 8, 11, and 14) 0.20 micrometers. Thereby, it turns out that there is effectiveness which controls the whiskers of tin, so that the diffusion layer of tin-copper is thick.

[0034]

[Table 2]

## スズめっき条件とスズめっき厚、ホイスカ性評価結果

サンプル	1回目銀めっき厚	2回目めっき厚		ホイスカ観察結果			
		合金層厚	純スズ厚	30日	60日	90日	180日
1	0	0.22	0.35~0.4	0	0	0	0
2	0.01	0.15	0.25~0.3	2	5	10	15
3	↑	0.20	0.25~0.3	0	0	0	0
4	↑	0.25	0.25~0.3	0	0	0	0
5	0.05	0.15	0.25~0.3	1	6	11	17
6	↑	0.20	0.25~0.3	0	0	0	0
7	↑	0.25	0.25~0.3	0	0	0	0
8	0.10	0.15	0.25~0.3	3	7	10	25
9	↑	0.20	0.25~0.3	0	0	0	0
10	↑	0.25	0.25~0.3	0	0	0	0
11	0.15	0.15	0.15~0.2	2	7	20	31
12	↑	0.20	0.15~0.2	0	0	0	0
13	↑	0.25	0.15~0.2	0	0	0	0
14	0.20	0.15	0.10~0.15	4	12	28	36
15	↑	0.20	0.10~0.15	0	0	0	0
16	↑	0.25	0.10~0.15	0	0	0	0

[0035] Although the tape career of 25 micrometers of copper foil was used in the above-mentioned example, when it replaced with this and the same evaluation as the above was performed by the tape career of 10 micrometers of copper foil, the 1st \*\*\*\*\* thickness did not generate copper superfluous lysis in 0.10 micrometers or less.

[0036] Moreover, after performing gold or palladium plating to substrate plating similarly like the above-mentioned example, when it evaluated, the same result as Table 1 of the above-mentioned example and Table 2 was obtained.

[0037]

[Effect of the Invention] As explained above, according to this invention, the following outstanding effectiveness is acquired.

[0038] According to the tape career for semiconductor devices and its manufacture approach of this invention, on the circuit pattern of the copper foil given through the adhesives layer on the insulating film By applying a solder resist to the position except a part for the terminal area of said circuit pattern, after performing noble-metals plating, such as silver, gold, and palladium, forming a tinning layer in a part for said terminal area after that, and heat-treating after that A tin-copper alloy layer with a thickness of 0.20 micrometers or more and a pure tin layer with a thickness of 0.15-0.80 micrometers are formed.

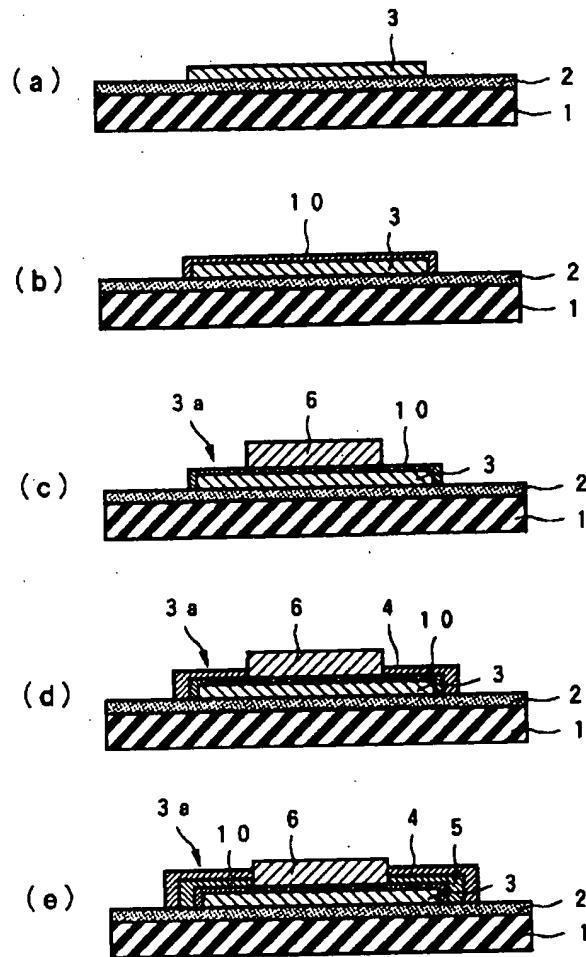
[0039] Noble-metals plating layers, such as silver, gold, and palladium, are formed previously, parts for a terminal area, such as a copper lead, are covered with this noble-metals plating layer, and a solder resist is formed in the part on that noble-metals plating layer. For this reason, since the copper front face is covered with the noble-metals plating layer and copper foil does not contact plating liquid even if plating liquid trespasses upon the inferior surface of tongue of a solder resist in the case of tinning processing, local electric corrosion does not happen. Therefore, the copper superfluous dissolution section is not formed in a copper lead. Therefore, it can lose un-arranging [ that the copper superfluous dissolution section exists in a copper lead, and the reinforcement of a copper lead becomes weaker ].

[0040] furthermore -- since the pure tin layer is set to 0.15-0.80 micrometers in the 2nd tinning processing -- the bonding nature of an inner lead -- good -- and plating -- who is not produced. Moreover, since the 2nd tin-copper alloy layer is set to 0.20 micrometers or more, sufficient whiskers

depressor effect can be acquired.

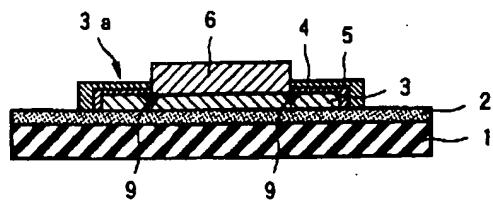
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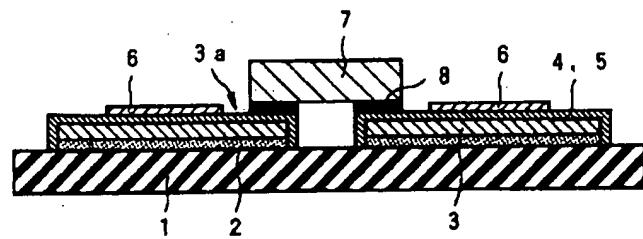
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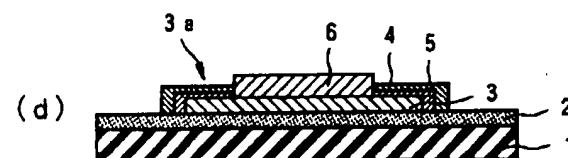
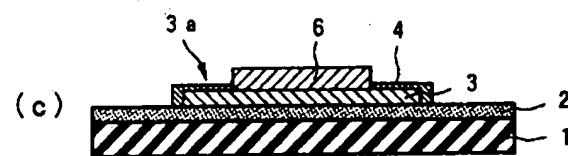
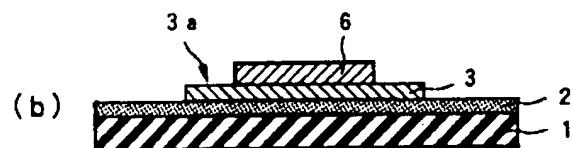


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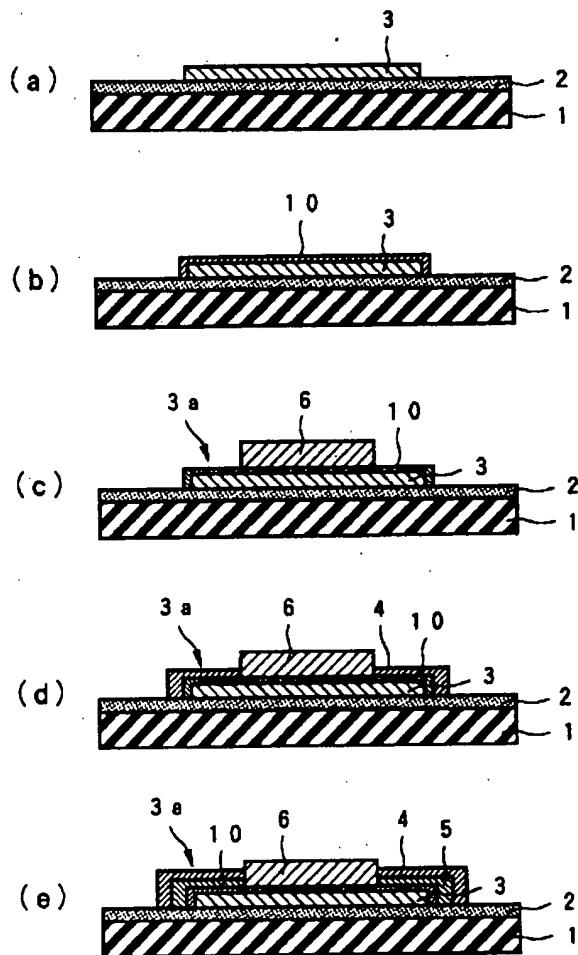






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[Translation done.]



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[Translation done.]